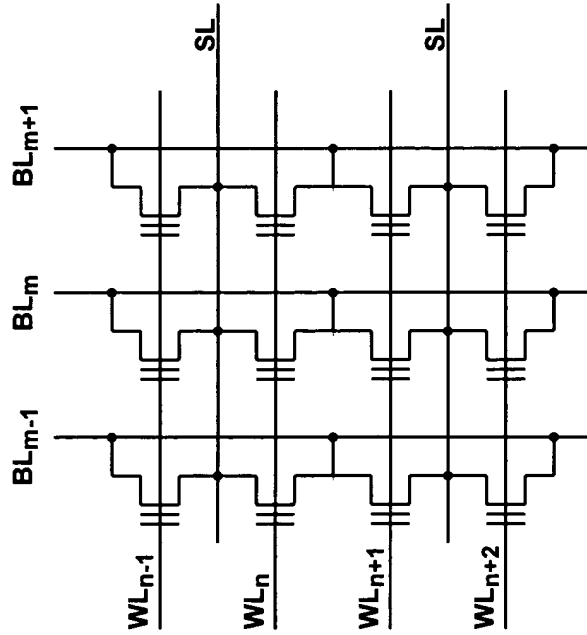


**A typical NOR-type Array
(showing Intel's ETOX Flash)**



WL = word line
BL = bit line
SL = source line
SG = select gate

NAND-type Array

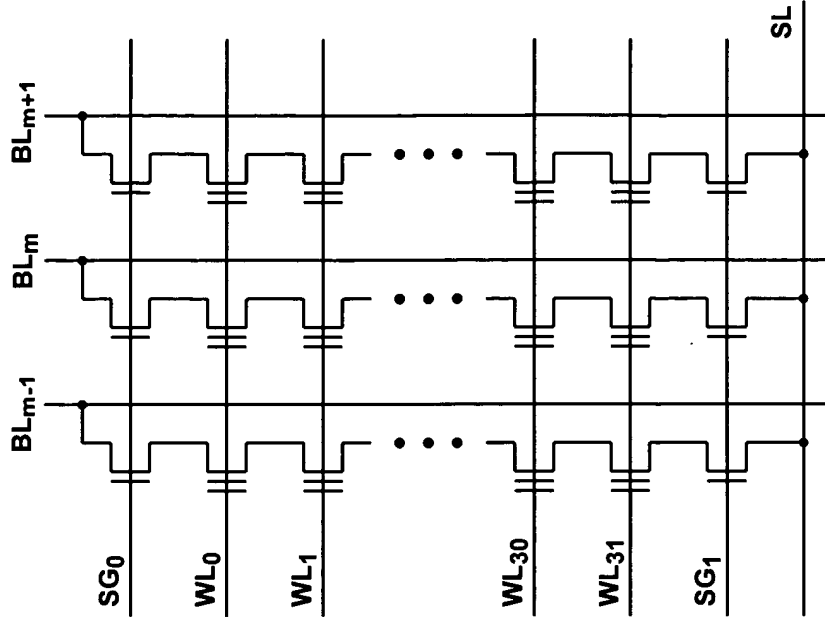
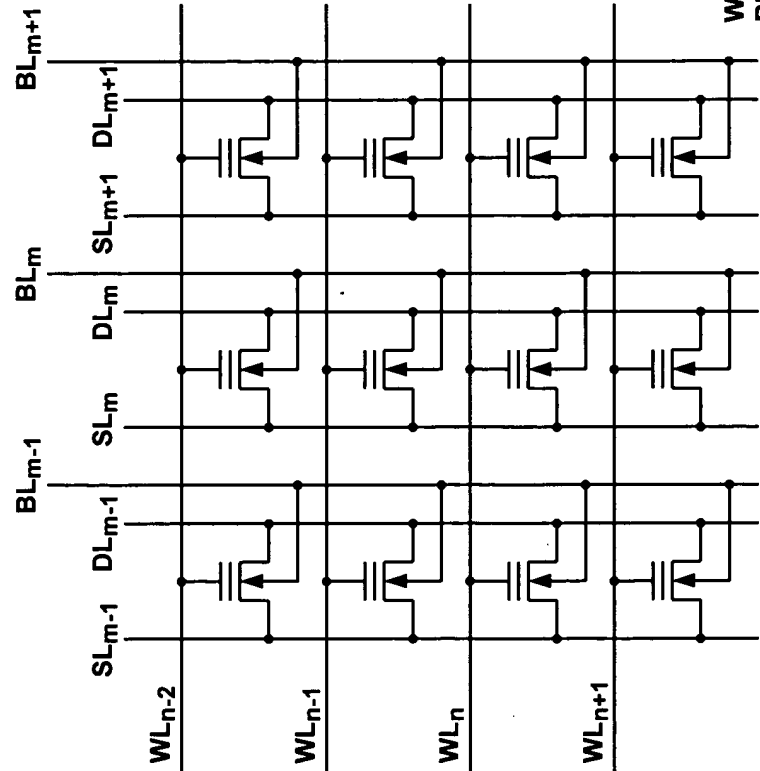


Fig. 1 NOR- and NAND-type Flash Arrays

Howe



**My invention is a NOR-type array
(also shown in Fig. 7 of my application)**



**The APA is a NOR-type array (also
shown in Fig. 8 of #5,796,142)**

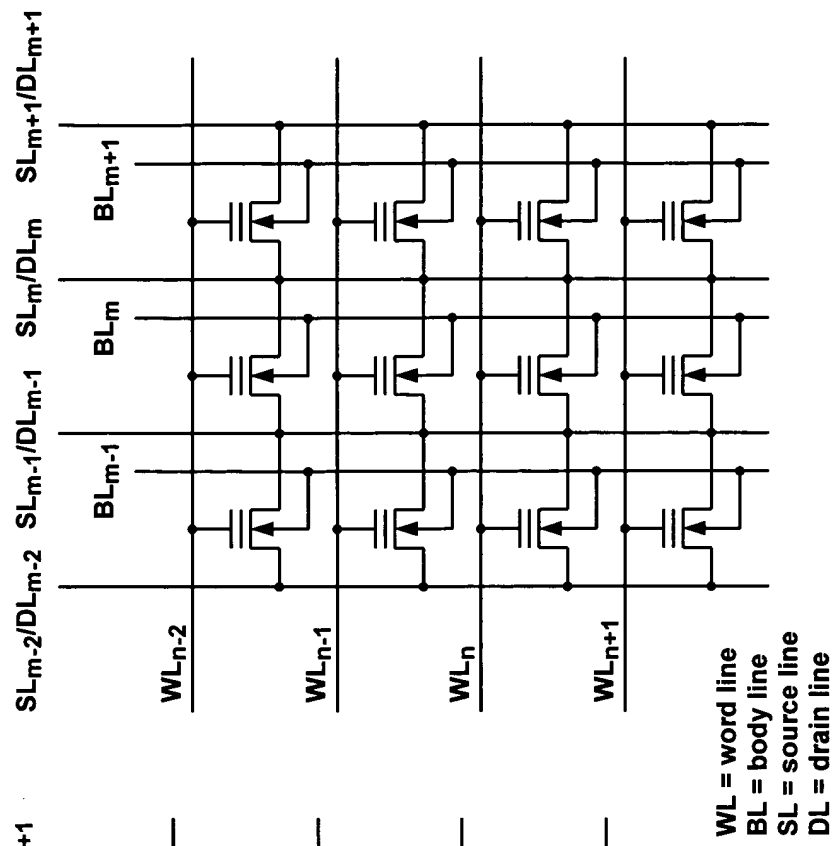


Fig. 2 Both my invention and the APA are contactless NOR-type arrays

Kouyama



What is claimed is:

- 201.** A semiconductor device having an electrically erasable programmable read only memory (EEPROM), comprising
- a contactless array of EEPROM memory cells disposed in rows and columns and constructed over a silicon-on-insulator wafer, each EEPROM memory cell comprising a drain region, a source region, a gate region, and a body region;
 - a plurality of gate lines each connecting the gate regions of a row of EEPROM memory cells;
 - a plurality of source lines each connecting the source regions and the body regions of a column of EEPROM memory cells; and
 - a plurality of drain lines each connecting the drain regions of a column of EEPROM memory cells;
- wherein the source lines and the drain lines are buried lines; and the source regions and the drain regions of a column of EEPROM memory cells are insulated from the source regions and the drain regions of the adjacent columns of EEPROM memory cells.
- 212.** The semiconductor device of claim **201**, further comprising at least a plurality of body lines each connecting the body regions of a column of EEPROM memory cells wherein the source line of a column of EEPROM memory cells is electrically connected to the body line of the same column of EEPROM memory cells.
- 223.** The semiconductor device of claim **212**, wherein the source line and the body line of a column of EEPROM memory cells are electrically connected by butting contacts.
- 74.** The semiconductor device of claim **1**, wherein at least one source line of a column of EEPROM memory cells is electrically connected to the body line of the same column of EEPROM memory cells.
- 85.** The semiconductor device of claim **74**, wherein the source line and the body line are electrically connected by butting contacts.